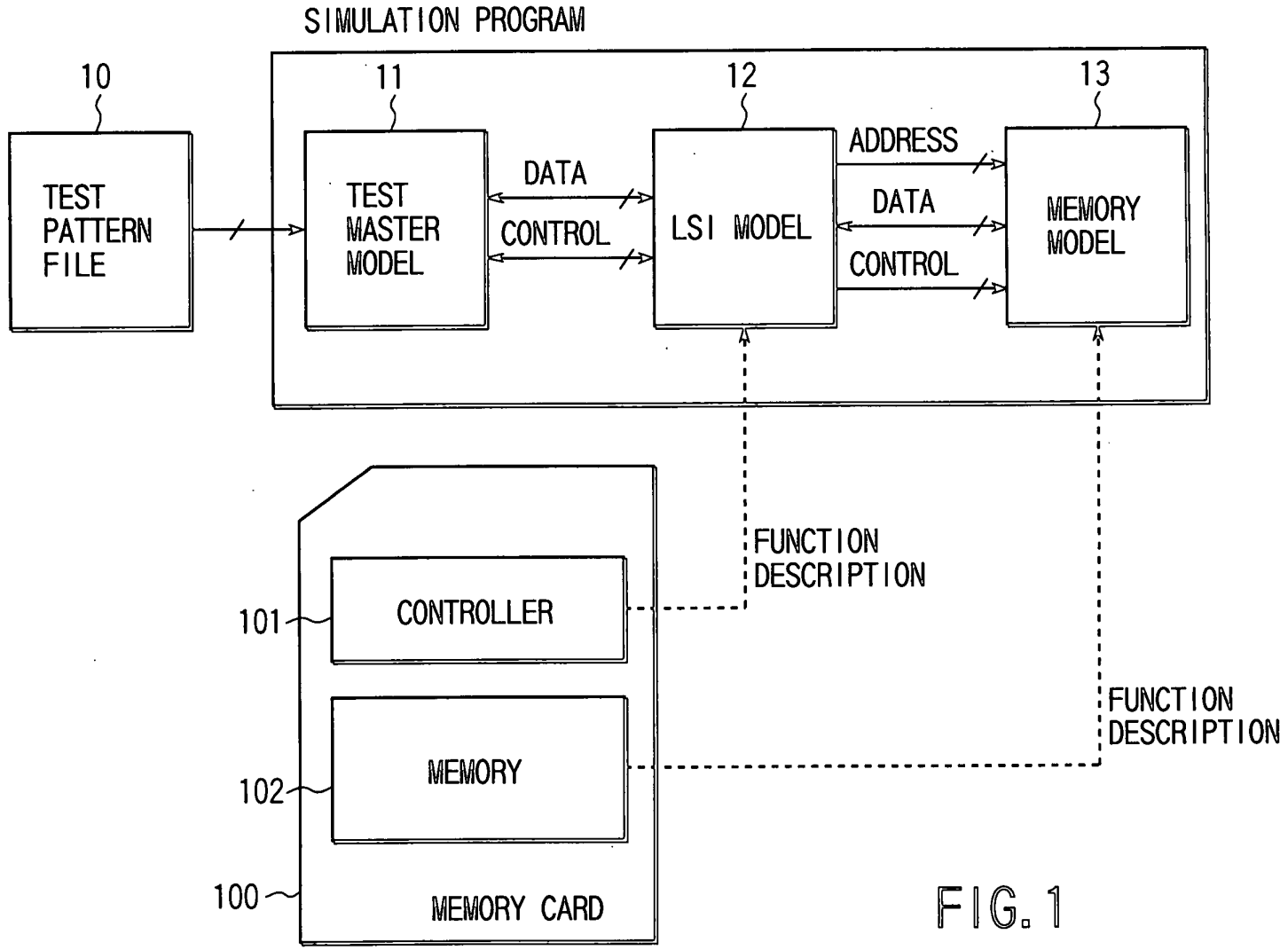
SIMULATION PROGRAM
10
11
12
13
TEST PATTERN FILE
TEST MASTER MODEL
DATA
CONTROL
LSI MODEL
ADDRESS
DATA
CONTROL
MEMORY MODEL
FUNCTION DESCRIPTION
FUNCTION DESCRIPTION
101
CONTROLLER
102
MEMORY
100
MEMORY CARD

FIG. 1

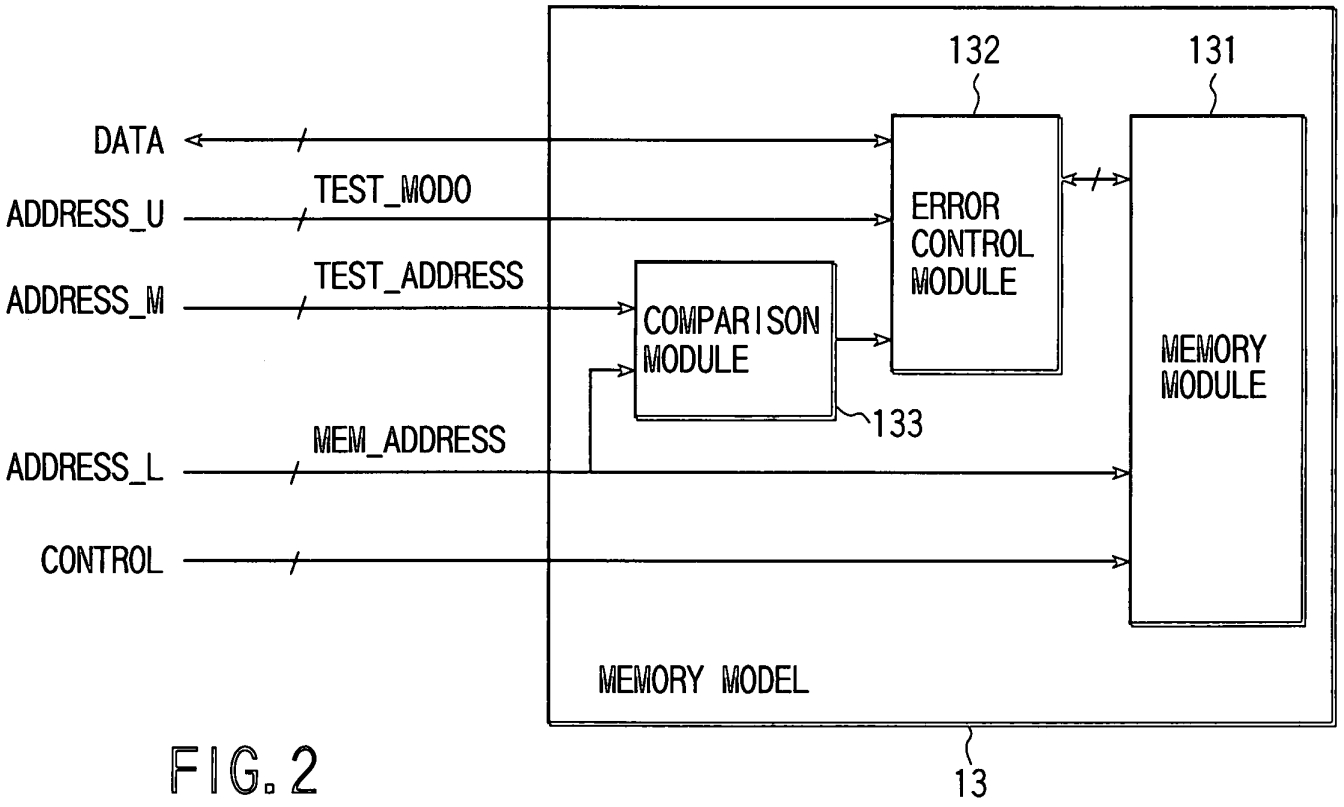

FIG. 2

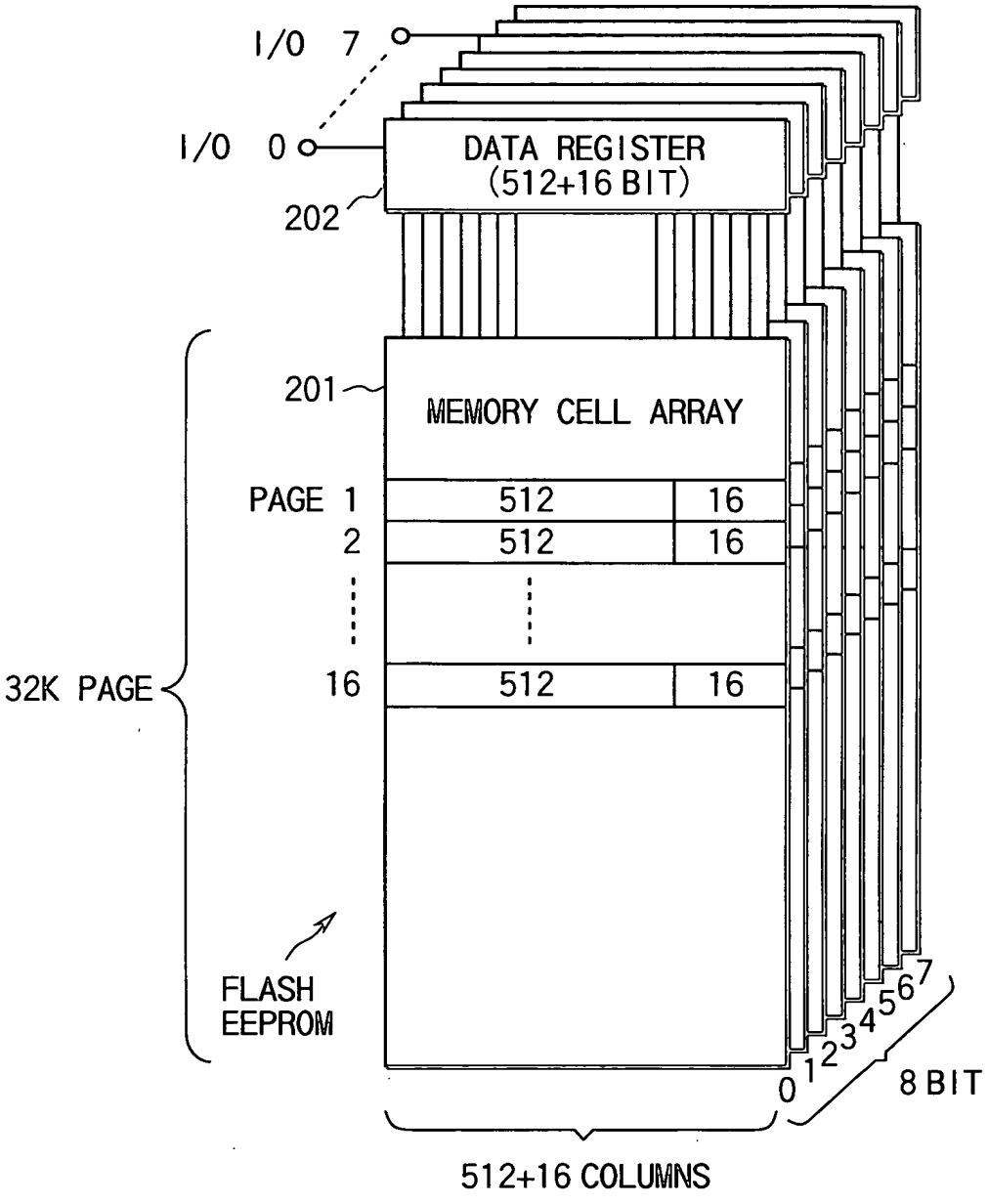
I/O 7
I/O 0
DATA REGISTER
(512+16 BIT)
202
201
MEMORY CELL ARRAY
PAGE 1
2
16
512
16
32K PAGE
FLASH
EEPROM
0 1 2 3 4 5 6 7
8 BIT
512+16 COLUMNS

FIG. 3

PAGE 1	ECC
2	ECC
3	ECC
4	ECC

FIG. 4

	TMA		TEST_ADDR		PA	MA
NAND ADDRESS	23:22	21	20:12	11	10:09	08:00
NORMAL	00	*	*	*	PAGE SELECT	COLUMN ADDRESS
FAIL	FAIL MODE	*	FAIL ADDRESS	*	PAGE SELECT	COLUMN ADDRESS

FIG. 5

W/R	NAND ADDRESS <23:22>	MODE	FAIL DATA
WRITE	00	PASS	NORMAL
	01	1 BIT_FAIL	DATA <07> IS INVERT
	10	2 BIT_FAIL	DATA <07:06> IS INVERT
	11	3 BIT_FAIL	DATA <07:05> IS INVERT
READ	00	PASS	NORMAL
	01	1 BIT_FAIL	DATA <07> IS INVERT
	10	2 BIT_FAIL	DATA <07:06> IS INVERT
	11	3 BIT_FAIL	DATA <07:05> IS INVERT

FIG. 6

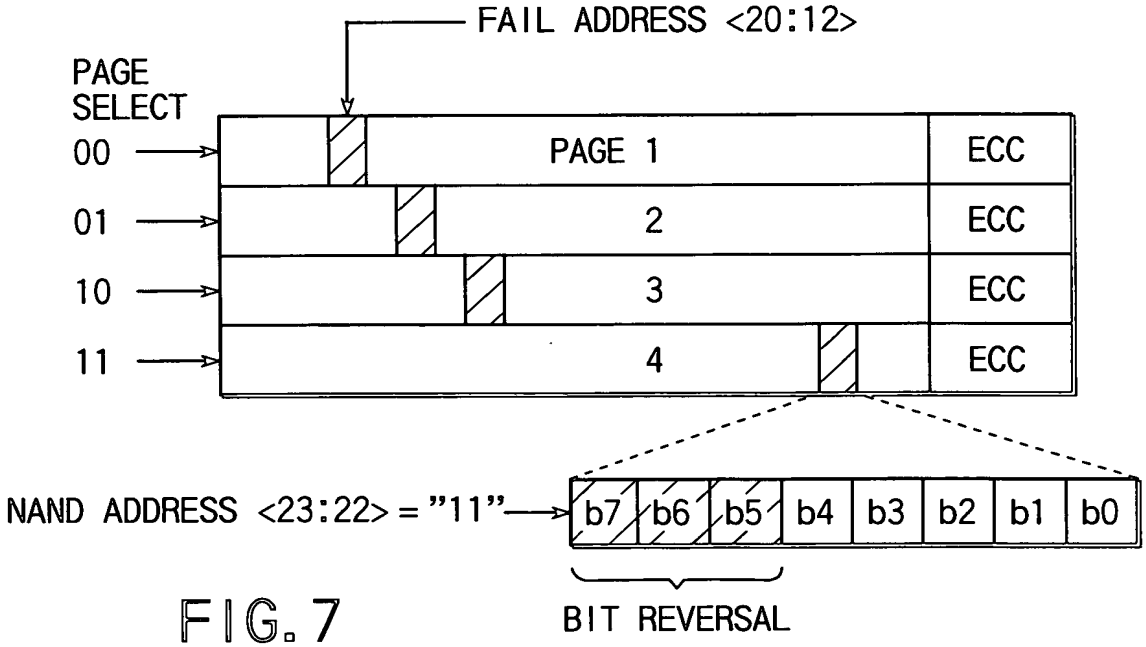

FIG. 7

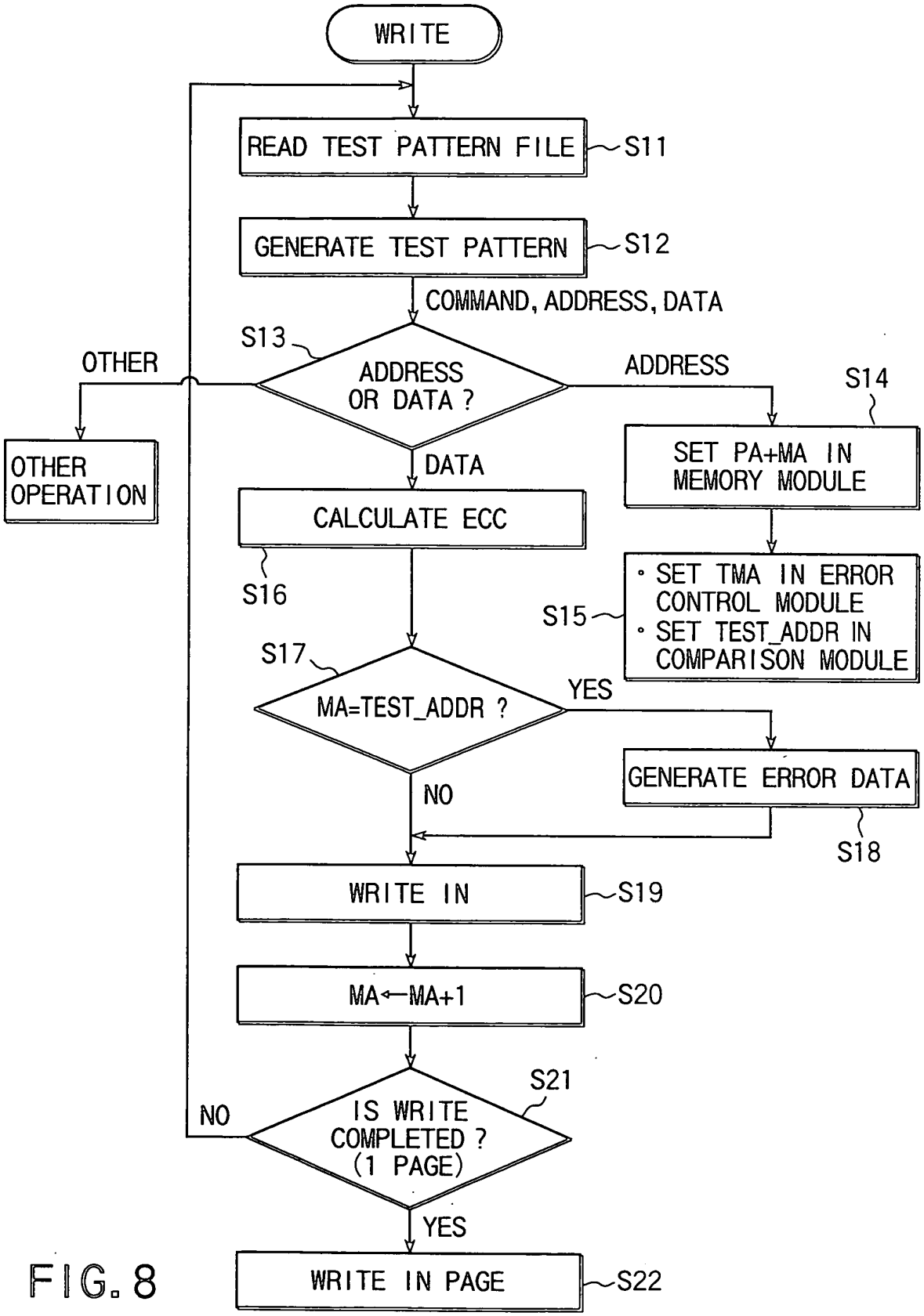
WRITE
READ TEST PATTERN FILE
S11
GENERATE TEST PATTERN
S12
COMMAND, ADDRESS, DATA
S13
ADDRESS OR DATA ?
OTHER
ADDRESS
DATA
OTHER OPERATION
S14
SET PA+MA IN MEMORY MODULE
CALCULATE ECC
S16
S15
• SET TMA IN ERROR CONTROL MODULE
• SET TEST_ADDR IN COMPARISON MODULE
S17
MA=TEST_ADDR ?
YES
NO
GENERATE ERROR DATA
S18
WRITE IN
S19
MA←MA+1
S20
S21
IS WRITE COMPLETED ? (1 PAGE)
NO
YES
WRITE IN PAGE
S22

FIG. 8

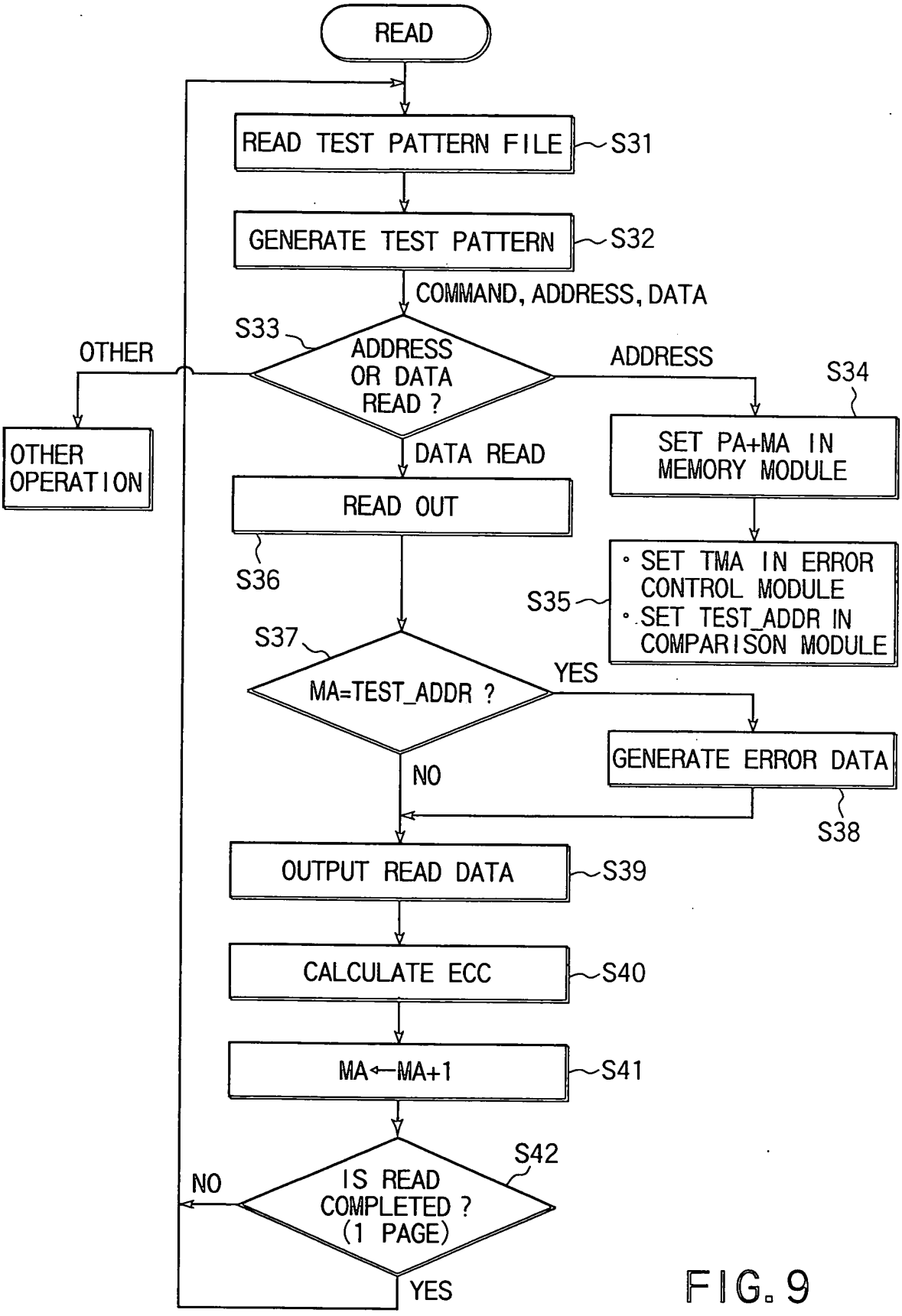
READ
READ TEST PATTERN FILE
S31
GENERATE TEST PATTERN
S32
COMMAND, ADDRESS, DATA
S33
ADDRESS OR DATA READ ?
OTHER
OTHER OPERATION
ADDRESS
S34
SET PA+MA IN MEMORY MODULE
DATA READ
READ OUT
S36
S35
◦ SET TMA IN ERROR CONTROL MODULE
◦ SET TEST_ADDR IN COMPARISON MODULE
S37
MA=TEST_ADDR ?
YES
GENERATE ERROR DATA
S38
NO
OUTPUT READ DATA
S39
CALCULATE ECC
S40
MA←MA+1
S41
S42
IS READ COMPLETED ? (1 PAGE)
NO
YES

FIG. 9